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AContinuous Time Delta Sigma Band Pass Modulator

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Abstract-
This paper presents the design of a CMOS fourth-order band pass sigma-delta modulator clocking at 280 MHz for direct conversion of narrowband signals at 70 MHz. The continuous-time loop filter is based on Gm-C resonators. A novel transconductance amplifier has been developed with high linearity at high frequency. The fourth-order modulator is implemented using 0.18 µm triple metal standard analog CMOS technology.Simulation in CADENCE demonstrates that the modulator achieves a SNR of 55 dB (~9 bit) performance over a 5 MHz bandwidth. The modulator's power consumption is 25 mWfrom supply power of ±1.8V.
Keywords: Analog and Mixed Signal IC Design, Analog-to-digital conversion, bandpassdelta sigma modulator, continuous-time, loop filter using Operational TransconductanceAmplifiers(OTA).

I. INTRODUCTION

With growing demand for wireless communication, the integrated circuit design for radio-frequency (RF) communication receivers has focused on high level of integration with small size, low power and low cost. To achieve these goals, the incoming radio frequency signals must be digitized. There are two RF receiver architectures where the onchip solutions are practical: direct conversion and super heterodyne conversion.

Digital IF receiver makes the low frequency operations, such as the second mixing and channel filtering in superheterodyne receiver, more efficient in the digital domain. The digital demodulation not only eliminates the I/Q mismatch problem inherent in analog demodulators but also provides more flexibility for the implementation of multi-mode functionality [2]. With the current technology developments, the size and power consumption will be scaled down. The digital IF architecture requires A/D conversion operating at high frequency, which is limited by linearity and dynamic range requirements due to the possible large adjacent interferes.

Bandpass sigma-delta modulators combine oversampling and noise shaping to get very high resolution in a limited bandwidth. They are widely used in applications that require narrowband high-resolution conversion at high frequencies. In recent years interests have been seen in wireless system and software radio using sigma-delta modulators to digitize signals near the front end of radio receivers. Such applications necessitate clocking the modulators at a high frequency (MHz or above). Therefore a loop filter is required in continuous-time circuits (e.g., using transconductors and integrators) rather than discrete time circuits (e.g., using switched capacitors) where the maximum clocking rate is limited by the bandwidth of Opamp, switch's speed and settling-time of the circuitry.

The specifications of the ADC for high-IF receiver are shown in Table 1.1. With no specific location of the intermediate frequency in all wireless standards, a 70 MHz frequency was chosen to avoid the effects of flicker noise as well as to push the state of art for the ADC design in CMOS 0.18um technology. With fs/4 architecture, the sampling frequency is set to 280MHz, a factor of 4 of the operational frequency. The 5 MHz bandwidth and 9 bit resolution were selected to accommodate the bandwidth and resolution requirements for video applications. Based on these requirements, a 4th-order bandpass continuous-time sigma delta modulator achieving a peak SNR of 55dB when measured in 5 MHz bandwidth is presented.

Table 1.1: Specifications of the CT BP ΣΔ modulator

Specification	**Value**
IF Signal frequency	70MHz(Fs/4)
Clock frequency	280MHz
Signal bandwidth	5MHz
Target SNR	>50dB
Technology	0.18um CMOS technology

II. Continuoustime bandpass sigma delta modulator architecture

The choice of the sigma delta ADC architecture depends on tradeoff between maximum signal to noise ratio (SNR) that can be obtained and the limited signal swing at all internal nodes (related to stability). The main architectural level choices for the ADC that affects its performance include the following: Order of the ADC (order of the loop filter), Single-loop or MASH (multi-stage noise shaping), Single-bit or multi-bit (number of comparator bits).

A fourth order, single-loop and 1-bit quantizer architecture is chosen for the CT BP sigma delta ADC implementation, which results in an optimum tradeoff between signal swing and SNR. A higher order loop filter increases the SNR, but it could suffer from potential stability problems as large signal swing may saturate the internal nodes.

According to Nyquist theorem, the center frequency of the CT BP sigma delta ADC can be placed at any frequency between DC and $F_s/2$, where F_s is the sampling frequency of the clock. The input signals are located around center frequency F_o with bandwidth Fin, and the choice of the ratio F_o/F_s is a tradeoff among sampling frequency (related to speed of the whole system), anti-aliasing filter requirements and the OSR [47]. The optimal solution to the problem is to place the center frequency (F_o) at one-fourth of the sampling frequency. This selection of clock frequency offers two main advantages. The first advantage is that the loop filter implementation becomes simple by using the low pass to bandpass transformation ($z \rightarrow z^{-2}$). The second advantage is that the digital demodulation I/Q signals becomes easy as it involves simple multiplication by {1,0,-1}. The OSR (defined as Fs/[2*Fin] for the BP sigma delta modulator) of the ADC is fixed by the choice of the sampling frequency.

The choice of architecture and the noise transfer function (NTF) of the ADC depends on the bandwidth specifications of the ADC. The quantization noise is attenuated by the notch NTF as long as it is the dominant noise source at the output, which is true when a narrow bandwidth is under consideration. For a wide bandwidth system, the integrated thermal noise floor will have a higher level than the quantization noise which necessitates a different design approach for obtaining the best SNR. The zeros of the NTF are all placed at a single frequency (center frequency of the filter) for a narrow bandwidth ADC, which ensures maximum possible reduction of the noise at the center frequency. The zeros of the NTF can be spread over the entire bandwidth for a wide bandwidth system, which results in an almost flat transfer function (combination of several closely spaced shallow notch functions) in the bandwidth of interest. Multi-bit comparator designs are also commonly used in wideband architectures at the cost of more power consumption.

There are three types of DACs return-to-zero (RZ), Half return-to-zero (HRZ) and Non return to zero(NRZ). Any two types of DAC's can be used to implement H(s). RZ and HRZ DAC waveforms are beneficial for reducing inter symbol interference and excess delay problems, so we might prefer them over NRZ DACs. As well, multi feedback BP modulators use both RZ and HRZ DACs in the same circuit.

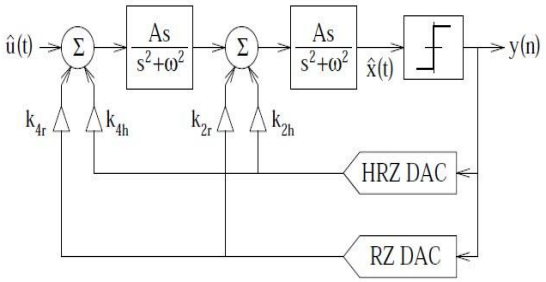

Figure 2.1 Block diagram for BP CT ΣΔ modulator

By comparing RZ DAC coefficients (k2r, k4r) and HRZ DAC coefficients (k2h, k4h) are obtained and this coefficients are scaled for improving SNR and noise shaping.

Table 2.1 Feedback coefficients of CT-BP ΣΔ modulator

Coefficients	**Value**
K4r	2.6815
K4h	-1.1107
K2r	-1.7547
K2h	3.1109

The Simulink model for 4th order bandpass modulator is shown in Figure 2.2. Design is implemented using SIMSIDES toolbox. Res_gmC_1pole is a block of resonator based on Gm-C integrators. Real_DAC_pulse_typesblock used for generating various types of pulses like Return to zero(RZ), Half return to zero(HRZ) and Non-return to zero(NRZ). RZ and HRZ pulses are used for implementing feedback coefficients shown in model below.

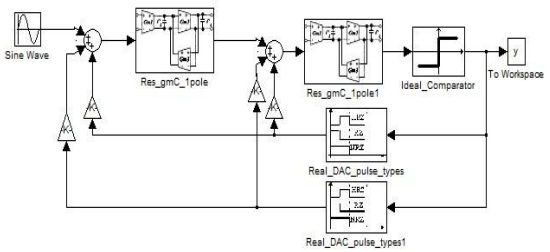

Figure 2.2 Simulink model for 4rth order CT Bandpass ΣΔ modulator using SIMSIDES

III. CIRCUIT DESIGN AND IMPLEMENTATION

Fully differential structure is used to implement the bandpass loop filter because of its good common-mode noise rejection, distortion performance and double output swing. Fig. 3.1 below. Shows the typical structure of the fourth-order resonator by using Gm-C topology.

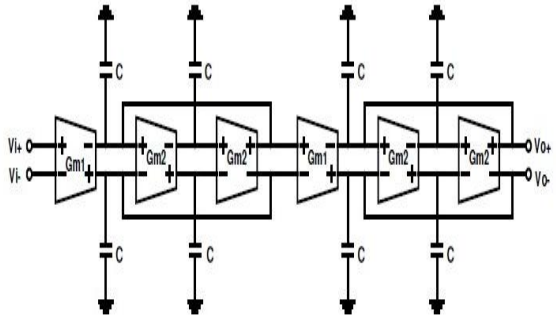

Figure 3.1 4th-order resonator

The center frequency of this resonator is determined by $gm2 /C$.

Simulation results of resonator,

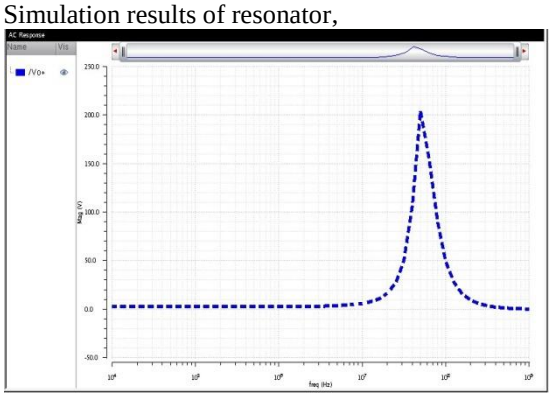

Figure 3.2 AC Magnitude response of a Resonator

IV. System Simulations

In this chapter the complete system is simulated at the schematic level. The performance of the 4th-order continuous-time bandpass modulator will be demonstrated. The continuous-time bandpass sigma delta modulator, shown in Figure 6.1 has been designed and simulated in 180nm complementary metal oxide semiconductor (CMOS) technology.

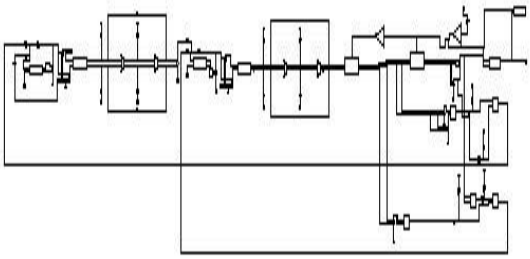

Figure 4.1 (a) Complete schematic of bandpass modulator

Figure 4.2 shows the transient response of continuous time Bandpass sigma delta modulator for thesine input of frequency 70MHz and 125mV p-p sine wave input signal.

Output of the modulator is pulse width modulated signal for 280 MHz clock frequency.

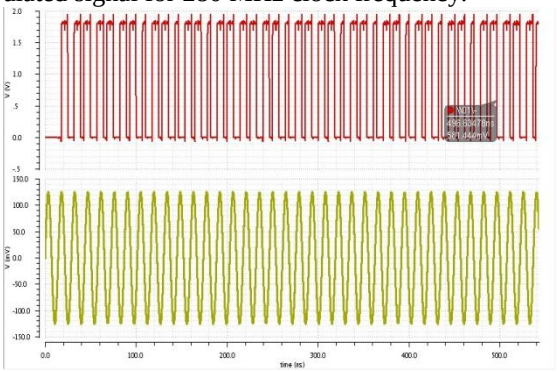

Figure 4.2 Transient response of the modulator

The below output spectrum is generated by exporting the bit file from cadence to matlab and plotting the fast fourier transform (FFT) using blackman window. FFT of quantizer output plotted for $N=2^{16}$ points is shown in figure 4.3.It took almost six hours to generate the bit stream. From this plot obtained SNR of the modulator is 55dB and resolution ENOB is 9 bits. As can be seen in fig 6.4 the spectrum of the designed modulator is a typical bandpass curve with signal in between the noise floor. Figure 4.4 shows the zoom in image of figure 4.3.The signal peak can be seen at centre frequency of 70MHz and the curve shows typical bandpass characteristic with signal between the noise floor.

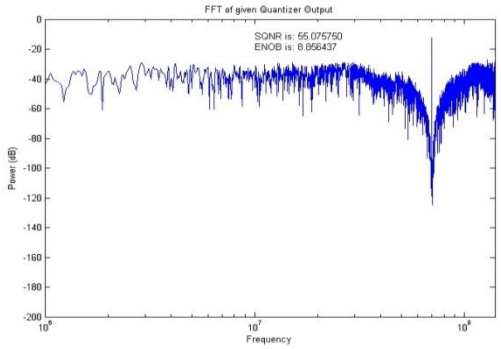

Figure 4.3 FFT of Quantizer output

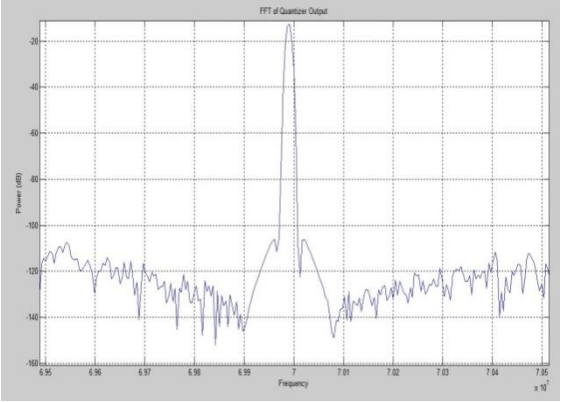

Figure 4.4 FFT of the Quantizer output zoomed in to show the signal peak at 70MHz.

V. Conclusion and Future scope

The strong growth in the wireless communications industry has led to the development of a large number of wireless standards for various market segments (cell phones, wireless networking, global positioning etc.). The main requirement of the next generation wireless devices is the support of multiple standards on the same chipset with negligible increase in power consumption and this issue is addressed in this work.

The design of a fourth order CT BP sigma delta ADC based on GmC filters for direct IF digitization at 70 MHz center frequency has been modelled, designed and simulated in 180nm CMOS technology. Operational transconductance amplifier was proposed using techniques like source degeneration using resistors and cross coupling. The input operational transconductance amplifier achieves gain of 24.1dB,transconductance of 3.69mA/V and IM3 of -65dB.The second operational transconductance amplifier has a gain of approximately 35dB,transconductance of 3.88mA/V and IM3 of -70dB.Using the input operational transconductance amplifier and high gain operational transconductance amplifier resonator was designed. Because of improved performance of both the operational transconductance amplifier there has been significant improvement in resonator performance and in turn in continuous time band pass sigma delta parameters like Signal to noise ratio(SNR),bandwidth and resolution.

The bandpass modulator can be clocked at a much higher frequency for direct conversion of signals greater than 70MHz.The modulator's signal to noise ratio(SNR) and bandwidth can be improved so that it can be used for other wireless standards. The most important block of modulator is resonator. Quality factor of resonator can be enhanced to improve modulator performance.

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